# Bakshree Mishra

bakshree.cs.illinois.edu | bmishra3@illinois.edu | linkedin.com/in/bakshree

## Education

**PhD in Computer Science** **2021-Present**
University of Illinois, Urbana-Champaign
Advisor: Prof. Sarita Adve
Area of Interest: Machine Learning and Computer Architecture, MLSys
GPA: **3.9/4**

**M.Tech in Computer Science** **2015-2017**
National Institute Of Technology, Rourkela
Advisors: Prof. Bansidhar Majhi (NIT Rourkela), Mr. Tarjinder Singh (Intel)
GPA: **9.69/10**

**B.Tech in Computer Science and Engineering** **2010-2014**
College Of Engineering and Technology, Bhubaneswar
GPA: **8.85/10**

## Publications

**Mishra, B.** and Chakraborty, D. and Makkadayil, S. and Patil, S. D. and Nallani, B. *Hardware Acceleration of Computer Vision and Deep Learning Algorithms on the Edge using OpenCL*, appeared in the Proceedings of EAI Endorsed Transactions on Cloud Systems, 2019 [Paper]

## Patent Applications

Singh, T., Sridhar, S. R., Sumiran, R., **Mishra, B.**, Makkadayil, S., Thyagarajan, V., and Baireddy, V., Intel Corp, 2022. *Graph Reordering and Tiling Techniques.* U.S. Patent Application No. **17/533,976**

Makkadayil, S., Paul, S., Saifee, S., **Mishra, B.**, Thyagarajan, V., Velayudha, M., Khellah, M. and Udofia, A., Intel Corp, 2021. *Parallel pruning and batch sorting for similarity search accelerators.* U.S. Patent Application **17/358,495**

Boschi, G., Makkadayil, S., Manjunath, R., **Mishra, B.** and Campinoti, A., Intel Corp, 2021. *Register fault detector.* U.S. Patent Application **17/353,848**

## Research

**Hardware acceleration with heterogeneous disaggregate accelerator systems** June 2022 – Present
- Created a synthetic accelerator benchmark suite to evaluate algorithm/accelerator system behavior
- Co-developed a light-weight accelerator synchronization interface in RTL
- Analyzed impact of composable accelerator systems in accelerating spatial audio, mini-ERA and FCNNs

**Evaluation of Spandex Coherence Protocol** August 2021 – June 2022
- Converted mini-Era workload to baremetal for evaluation on Xilinx FPGA using ESP workflow
- Implemented sensor-simulation in cpu tiles and collected performance numbers

## Projects

**Real-Time Barcode Localization and Detection on Edge Devices**
- Industrial problem which required decoding barcode on fast moving objects from camera feed
- Created custom accelerator for the algorithm bottleneck, Barcode localization, using OpenCL HLS
- Highly pipelined architecture leveraging data redundancy in algorithm
- Improved performance from **19 FPS** to **104 FPS** on 2MP video to satisfy industrial constraints
- **Paper** accepted at Intel Design and Test Technology Conference (DTTC), 2019

**Real-Time Optical Character Recognition on Edge Devices**
- Created CNN topology and trained on in-house character image dataset
- Created OpenCL based FPGA accelerator having parallel convolution engines and buffered partial results
- Accelerator improved performance from detected 250 characters at **10 FPS** to **50 FPS** from 2MP video
- Presented **live demo** at Intel DTTC, Portland, OR, 2019
- **Paper** presented at IEEE WinTechCon, Bangalore, India, 2019

**Hardware Design for Functional Safety IP**
- Learnt traditional HW design using RTL to implement Fault Detector module for Functional Safety (FuSa)
- Went through High Level as well as Micro Architecture Specifications for designing hardware
- The IP achieved ISO26262 certification for Functional Safety
- **Paper** on our work was accepted at Intel DTTC 2019

**System on Chip (SoC) for CV/ML Acceleration**
- Modelled SoC on Hybrid-FPGA platform after reviewing internal and third party architecture specifications
- Booted OS on H-FPGA platform successfully and enabled early FW and SW development
- Found critical bug in bootloader code impacting secure boot
- Co-architected an accelerator IP to handle similarity search workloads in the SOC for machine learning

**Real-Time Pedestrian Detection System Using OpenCL-Based FPGA Acceleration**
- Created a custom architecture for computer vision based Pedestrian Detection system for Master's research
- Deep-dived into FPGA OpenCL compiler optimization issues and found impactful solutions
- Independently improved initial design to give **3x** performance while reducing area by **10x**

**Context-Aware Voice Assistant**
- Created an always on, context-aware NLP agent to offer recommendations instead of executing commands
- Trained Bi-LSTM based SLU algorithm to understand context over conversations and multiple sentences
- Used Mycroft framework to create end-to-end Voice Assistant as proof of concept

## Select Awards and Honors

- Among Teachers Ranked as Excellent for CS225 in Spring 2022 — 2022
- Best Paper in Track Award, Intel HSPE TechCon 2021 — 2021
- Multiple Intel Division and Department Recognition Awards (2017-2021) — 2021
- 2nd Runners' Up in Intel India WIN Hackathon — 2017
- 2nd rank holder in CS Department (out of ~110 students) at NIT Rourkela — 2017
- CET Merit Scholarship (Undergrad scholarship 2010-2014) — 2010
- Selected for National Talent Search Examination Scholarship — 2008
- Rajiv Gandhi Chhatra Prativa Award for securing 8th rank in State, Xth CBSE Boards — 2008

## Work Experience

**Graduate Research Assistant** — May 2022 – Present
Workload analysis on heterogeneous platforms — *University of Illinois, Urbana Champaign*

**Graduate Teaching Assistant** — August 2021 – May 2022
CS 233 Computer Architecture, CS 225 Data Structures — *University of Illinois, Urbana Champaign*

**Design Engineer** — June 2017 – August 2021
Analysis and acceleration of Machine Learning Algorithms — *Intel Corporation, Bangalore*

**Graduate Technical Intern** — May 2016 – May 2017
Acceleration of Pedestrian Detection and other ADAS Algorithms — *Intel Corporation, Bangalore*

**Assistant System Engineer** — June 2014 – July 2015
Development of E-Municipality portal — *Tata Consultancy Services, Bhubaneswar*

**Summer Intern** — June 2013 – August 2013
Prototype modules for E-Municipality portal — *Tata Consultancy Services, Bhubaneswar*

## Technical Skills

- **Programming/Scripting Languages** — C/C++, Python, Shell Scripting, Java, C#, MATLAB, OpenCL
- **Tools** — Quartus, Design Compiler, Eclipse
- **Databases** — Oracle 10g, SQL Server

## Volunteering and Service

- Named one of Top 50 Volunteers in Intel India — 2020
- Regularly volunteer to conduct **music therapy** at a **Cancer Hospice**, Karunashraya — 2018 - 2021
- Won an Intel Seed Grant and oversaw renovation of **nurses' dining hall** at Karunashraya — 2019
- During undergrad, co-founded the student e-zine **CET Rising**, and served as **Chief Editor** — 2013 - 2014